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Design and Implementation of Controller for Car parking System using VHDL

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ABSTRACT –
Introduction: Presently multi day's vehicle parking is a basic issue and step by step its necessity is expanding. In Bangladesh we are as yet utilizing the manual vehicle parking framework and that is the reason, we are confronting issues like wastage of time and fuel discovering free space around the parking ground when we have to park our vehicle which requires a decent measure of lighting. Another issue is clutter that occurs while parking on the grounds that there is no specific framework anybody can park anyplace that at some point makes harm the vehicles while moving out or in the parking area. Security is likewise an issue there. To tackle these issues, we are exhibiting new vehicle parking system. The system fills in as pursues: where the quantity of accessible stopping spaces will be shown in the LED display. While stopping out the driver should give the code to the administrator at the leave gate. The work presented in this paper gives more insight and deeper understanding of constituting modules of parking system. This paper investigates the optimized parking system through FPGA employing "logic forgathers" including multiple registers as their logic block. And we show that this algorithm is superior to an existing packing algorithm.

Keywords - FPGA, VHDL, IR Sensor, Relay, FSM

I. INTRODUCTION

The Car Parking Slot System is a technological solution designed to streamline and optimize the management of car parking spaces. With the increasing number of vehicles on the roads and the limited availability of parking spots, efficient parking management has become a crucial challenge in urban areas. This project aims to address this issue by developing an automated system that efficiently allocates and monitors parking slots in a parking facility.

The Car Parking Slot System utilizes various technologies such as sensors, microcontrollers, and a central control unit to automate and enhance the parking experience for both car owners and parking lot operators. By implementing this system, users can save time and effort in finding an available parking space, while parking administrators can efficiently manage and maximize the utilization of parking resources. Ramneet Kaur and Balwinder Singh [1] proposed a car parking system using FPGA. In this paper, LCD displays detect that whether the space is available or not. If space is available, then the door opens for the vehicle entrance. RF module is for transmitting and receiving area availability information. Khor Jing Yong and Muataz H. Salih designed and developed an embedded auto car parking system using FPGA for emergency conditions. This method can be used for the safety of the driver. . Bhavanachendika, Alapati Manideepu, Fazal Noorbasha [3] proposed a Secured car Parking System Using Verilog HDL. In this secured car

parking system when the car park in a particular place everyone will get a password or key which is required to take a car from slots. If the password or key is matched with the original then the gate will open otherwise it will remain lock or the buzzer will give a loud sound when the password is wrong. S. Sharmila Devi, Blessy Angel J.J.R., Deepa. and M., Kaaviya.A. I [4] designed a car parking system using FPGA. In this research, IR sensors are used to identify the car entering and exiting from the parking area.

How much free space is available was identified by fixing cameras. An ultrasonic sensor is used for the distance measured, number of

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vacant slots, and number of cars which already parked. M. M. Rashid, A. Musa, M. Ataur Rahman, and N. Farahana,A. Farhana [5] designed an Automatic Parking Management System.

This system is implemented using Matlab. Data is collected from ultrasonic sensors of each Parking space. If the parking space is no more than sign is displayed through LCD. In this system when the car is entering image is captured and entering time is also required. The plate reference number is also recorded. In this system when the car is entering image is captured and entering time is also required. The plate reference number is also recorded. Car image is captured because it's used in license plate number and entering time is for a fee of parking. RehanullahKhana, Yasir Ali Shahab, ZeeshanKhanc, KashifAhmedad, Muhammad Asif Manzoorc, Amjad Alia [6] developed an Intelligent Car Parking Management System On FPGA.Hua-Chun Tan; Jie Zhang; Xin-Chen Ye; HuiZe Li; Pei Zhu; Qing-Hua Zhao [7] proposed an Intelligent car-searching system for a large park area. Real time FPGA systems were implemented in Paper [8] and Paper [9]. Azeem Mohammed Abdul,

B. MmuraliKrishna, K.S. N Murthy, Habibulla khan, M. Yaswanth, G. Meghana and G.L. Madhumati [8] designed IOT Based Home Automation using Day by day our country has been advanced drastically, now we are in this state that we have a lot of well-constructed roads, commercial building and increasing number of automobiles. With the increasing number of roads and highways transportation has become the backbone of our day-to-day life. Transportation has also become the strength of our economy for its wide usage in trade and business. Hence, it has been a matter of thought to park these transportations and vehicles in safe places. We still use the very old-fashioned manual procedure of parking when it comes parking these vehicles. These are maintained in unplanned manner, without any discipline. Due to this system people can park their cars anywhere they want to, which creates a mess as people do not follow the discipline most of the time. While parking in and recovering car due mismanagement cars can get dent by bumping with each other as there is lack of sufficient space. This leads to arguments, fights among people which sometimes create traffic jam. This is also an economical lose as we need to repair our damaged car. Due to this disorder in parking our valuable time gets wasted. It harms the students, office going staffs and emergency patients to an excessive scope. It also causes economical loss to commercial places like shopping malls, amusement parks as people are more likely not to visit these places due to this parking hazard. Automated car parking systems will provide several benefits. It will save time and fuel cost. In manual parking system it is too hard to find out the vacant space for parking, it is very much time consuming. Sometimes it causes late in meeting or other important works. It will save fuel as in this system an automatic car parking the vehicle into the required slot. This will reduce the fuel cost of probing for parking space. Here we do not need to FPGA. Prasanna S. Bhoite and Madan B. Mali [9] developed Wireless Signal Transmission using an lighting all over the parking space all the time. It will only have the lights on when it moves and where is the path and it is very much electricity saving also. It provides security from theft of vehicle. It can introduce us to advanced digitalized systems which show us the Engineering excellence in our country.

Android Mobile and FPGA. Devchandra Singh and Dr Manoj Kumar [10] designed and developed a Bluetooth based home automation system using FPGA.

Key Features of the Basys 3 Board:

FPGA: The board features a Xilinx Artix-7 FPGA, which is a mid-range FPGA offering a good balance between performance and cost. The Artix-7 FPGA provides a high level of programmable logic cells, memory blocks, and DSP slices, allowing users to implement complex digital designs.

Fig 2. BASYS 3

We give the Basys 3 board the power from the USB port (J4). Source selection is done by using the jump switch (JP2). To turn the power supply on or off we use Power switch (SW16). LED glowing denotes the normal operation of supplies. External power supply of 5V can be given through the J6 near JP2.

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I/O Interfaces: The Basys 3 board offers a variety of I/O interfaces, including: 16 user switches: These switches can be used as inputs to the FPGA for different purposes, such as user inputs or configuration options [2].

16 user LEDs: These LEDs can be controlled by the FPGA to provide visual feedback or indicators.

Push-buttons: The buttons provide additional user inputs for interaction with the FPGA design.

4-digit seven-segment display: This display can be used to show numeric values or other alphanumeric characters.

VGA port: The board has a VGA port for connecting a monitor or display, allowing users to create graphical output from their FPGA designs.

USB-UART bridge: The USB-UART bridge enables communication between the board and a computer, making it easy to program the FPGA and exchange data.

PMOD connectors: The Basys 3 board has four PMOD connectors, which are standardized expansion ports for connecting various peripheral modules, such as sensors, communication modules, or motor controllers.

Programming and Configuration: The Basys 3 board can be programmed and configured using the Xilinx Vivado Design Suite. The suite provides a comprehensive development environment for FPGA

designs, including synthesis, simulation, implementation, and programming tools. The board can be programmed using a USB cable connected to the computer.

Educational Resources: Digilent provides a wealth of educational resources, tutorials, and example projects to support users in learning FPGA development with the Basys 3 board. These resources cover topics such as digital design, Verilog or VHDL programming, and FPGA implementation techniques.

Power Supply: The Basys 3 board can be powered either through the USB connection or an external power supply. It supports a wide input voltage range to accommodate various power sources [3].

VIVADO SOFTWARE:

Vivado Design Suite is a software tool developed by Xilinx, which is used for designing, implementing, and analyzing digital systems using hardware description languages (HDLs) like VHDL. Vivado supports FPGA (Field-Programmable Gate Array) and SoC (System-on-Chip) designs, providing a comprehensive platform for hardware development [4].

Here is an explanation of the key features and functionalities of Vivado Design Suite:
Design Entry: Vivado supports various methods for entering and designing your digital system. You can use the Vivado Integrated Design Environment (IDE) to create or import your design files written in VHDL. The IDE offers a user-friendly graphical interface where you can design and manage your project.

Synthesis: Once you have entered your design, Vivado's synthesis tool analyzes your VHDL code and converts it into a gate-level representation. It optimizes the design for area, performance, and power, generating a netlist that represents the internal structure of your digital system.

Implementation: In the implementation stage, Vivado maps the synthesized netlist onto the target FPGA or SoC device. It performs technology mapping, placement, and routing, assigning logic elements and interconnections to achieve the desired functionality. Vivado also handles timing constraints and optimizations to ensure proper operation of the design.

Simulation: Vivado provides a built-in simulator that allows you to verify and validate your VHDL design before synthesis and implementation. You can create testbenches to simulate the behavior of your design and check for correctness and functional accuracy. The simulator supports advanced debugging features for troubleshooting and waveform analysis.

Verification: Vivado offers various verification features to ensure the correctness of your design. It supports formal verification techniques, such as static timing analysis, to check for violations of timing constraints. You can also use the Vivado Integrated Logic Analyzer (ILA) to capture and analyze internal signals within your design for debugging purposes.

Debugging and Analysis: Vivado provides a range of debugging and analysis tools to help you

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identify and resolve issues in your VHDL design. It offers visual feedback through waveforms, timing diagrams, and resource utilization reports. You can also use the Vivado Tcl Console and Vivado Lab Edition for in-system debugging on hardware.

IP Integration: Vivado includes a vast library of pre-built IP (Intellectual Property) cores that you can integrate into your VHDL design. These IP cores provide ready-to-use functions and peripherals, saving design time and effort. Vivado also supports creating custom IP cores that can be reused in future designs.[5]

Design Constraints: Vivado allows you to specify design constraints using the Constraints Language (XDC), which helps in controlling the physical implementation and performance of your design. You can define constraints related to timing, placement, clocking, I/O, and other aspects to meet your design requirements.

System Integration: With Vivado, you can integrate multiple subsystems and IPs into a complete system design. It supports hierarchical design methodologies, allowing you to divide your design into manageable blocks and create interconnections between them. Vivado helps with system-level validation and integration.

Device Configuration and Programming: Once your design is complete, Vivado assists in configuring the target FPGA or programming the SoC device. It generates bitstream files that contain the configuration data for the device, which can be loaded onto the hardware for execution.

FPGA design:
FPGA (Field-Programmable Gate Array) design involves creating digital logic circuits or systems using programmable hardware devices. Unlike traditional integrated circuits, FPGAs can be reprogrammed or reconfigured to implement different functions or designs after manufacturing. This flexibility makes FPGAs popular in various fields, including digital signal processing, embedded systems, telecommunications, and high-performance computing.

Artyx family:
FPGA Architecture: FPGAs consist of a matrix of programmable logic blocks (PLBs) interconnected by a network of programmable routing resources. Each PLB contains lookup tables (LUTs) that can implement combinational logic functions, as well as flip-flops or registers for sequential logic. The routing resources allow signals to be routed between different logic blocks.

The Artyx family of FPGA is a series of development boards from Digilent that use the Xilinx Artix-7 FPGA chips. These boards are designed with versatility and flexibility in mind, and they have Arduino™ headers and multiple Pmod™ ports for easy expansion. The Artix-7 FPGA chips are part of the Xilinx 7 series of FPGAs, which offer high performance, low power consumption, and high integration[2]. The Artix-7 FPGA chips have up to 215K logic cells, up to 16 x 6.6G transceivers, up to 13Mb of block RAM, and support for DDR3-1066 memory. The Artyx family of FPGA boards can be used for various applications, such as software-defined radio, embedded vision, robotics, and IoT

.Artix-7 FPGA Development Board - Digilent Arty A7 - Xilinx. https://digilent.com/shop/arty-a7-100t-artix-7-fpga-development-board/.Artix 7 FPGA Family Xilinx. https://www.xilinx.com/products/silicon-devices/fpga/artix-7.html. How to Choose Xilinx Artix 7 FPGA With Full Part Number List. https://www.raypcb.com/artix-7-fpga-board/. Artix UltraScale+FPGA Family-Xilinx. https://www.xilinx.com/products/silicon-devices/fpga/artix-ultrascale-plus.html.

Field Programmable Gate Arrays (FPGA) are the semiconductors which are connected using programmable interconnectors. Therefore, the block diagram of FPGA consists of censors, controllers, memories, etc. Controllers used in FPGA are Sensor CMOS controller, Head Controller, Image capture Controller, External memory Controller. PCA algorithm (which is used where there are large number of features in our dataset) is also used in FPGA. CMOS sensors are used here which convert light into electrical signals. Then the connection is given to PC.

Design Entry: FPGA designs can be entered using hardware description languages (HDLs) such as VHDL (VHSIC Hardware Description Language) or Verilog. HDLs provide a textual representation of the desired digital circuit or system, allowing designers to describe the behavior and structure of the design.

Synthesis: After the design is entered in an HD synthesis tools are used to convert the high-level description into a gate-level representation. Synthesis involves mapping the HDL code to specific FPGA resources, such as LUTs and flip-

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flops, and optimizing the design for performance, area, or power consumption.

Place and Route: The place-and-route (P&R) process determines the physical locations of the design's logic elements within the FPGA and establishes the interconnections between them. P&R tools take into account the constraints provided by the designer, such as performance goals, pin assignments, and resource utilization, to generate an optimized layout and routing solution.

Timing Analysis: Timing analysis is performed to ensure that the design meets the required timing constraints. It checks the delays through the circuit and verifies that all signal paths can meet the specified performance requirements. Timing analysis helps identify and address potential timing violations, such as setup and hold time violations.

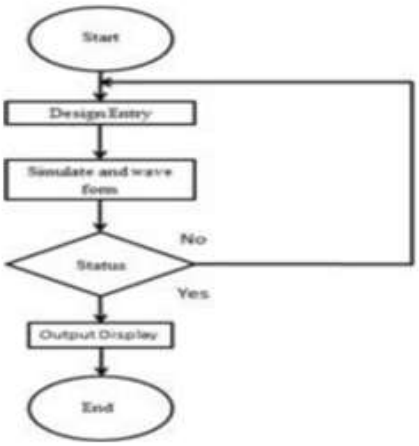
Simulation and Verification: Simulation is an essential step in FPGA design to verify the functionality and correctness of the design before synthesis and implementation. Simulation tools simulate the behavior of the design using test vectors or stimulus, allowing designers to validate the design's functionality and identify potential issues or bugs.

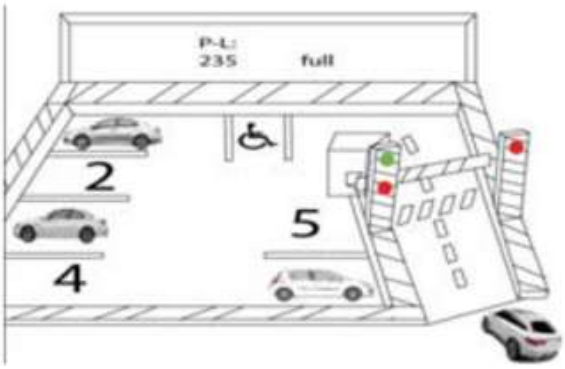
Implementation: Once the design is synthesized, the synthesized netlist is used to program or configure the FPGA device. The configuration bitstream, generated during the implementation process, contains the information needed to configure the FPGA with the desired logic functionality.

Debugging and Testing: After implementation, designers perform debugging and testing to ensure that the FPGA design operates correctly. This involves analyzing the behavior of the design, probing signals, and using debugging tools to identify and resolve any functional or performance issues.

FPGA Development Tools: FPGA development is supported by vendor-specific design tools, such as Xilinx Vivado, Intel Quartus Prime, or Lattice Diamond. These tools provide a complete design environment, including synthesis, simulation, implementation, and programming capabilities.[16]

II. METHODOLOGY:





In this chapter discuss about process and design of a car parking system.

This project consists of two parts, design a program and implement this with software. Quartus software was chosen for designing a program of the car parking system. In this software VHDL text editor is used to design of car parking system. After finish write a codding, continue with simulate to get wave form in software.[11]

The next important phase to undergo after conducting the study on the problem of tropical parking system is to identify the parking place situation. In a manual car parking system, there are a guard who direct the drivers to park their cars and drivers follow the guard's direction. Sometimes the guard directs them wrong for that reason collision with each other. It causes hamper the car and the car have to repair which mean a financial loss.

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Sometimes drivers injured seriously causes of this collision. Here we exhibit a car parking system in VHDL utilizing Finite State Machine (FSM). The VHDL code and test bench for the car parking system is utilize to create the procedure. The VHDL car parking system is appeared in the accompanying figure. There is a front sensor to recognize vehicles heading off to the gate of the car parking system. Another back sensor is to distinguish if the coming vehicle pass the entry way and getting into the car park. The goal of this project is to remove the car attendance, park the car safe and secured in a discipline way.

Developing Diagram and Interface Signal of Car Parking System

With the information given in above the inputs and outputs for the system can be accumulate through the interface known as State Machine. This Machine will process the inputs and executes those inputs in parallel with the outputs intended. In order to produce the intended outputs based on various conditions, the inputs needed to know the situation of car. The inputs include the clock to set the time, the reset and the sensors. Table 3.1 provides the list of both the inputs and the outputs for the State Machine with their description while Figure 3.3 illustrates the interface between inputs and outputs.[3]

Signal Name	Direction	Description
Clock	Input	Clock input to the state machine
Reset	Input	Reset signal to "reset' the state machine to a known state
Front Sensor	Input	Detect the coming vehicles
Back Sensor	Input	Detect the car into the car park
Password 1	Input	Gate is opened to let the car into the car park
Password 2	Input	If pass_1 is incorrect it will check again and let the car into the car park
Green LED	Output	FSM turns to RIGHT_PASS state; a Green LED will be blinking.
Red LED	Output	Wrong pass state and if the next car is coming before parking the current car then Red LED will be blinking
HEX 1	Output	Display 7-segment LED
HEX 2	Output	Display 7-segment LED

BCD TO 7 SEGMENTS:

BCD (Binary Coded Decimal) is a numerical representation system that uses a combination of four binary digits (bits) to represent each decimal digit from 0 to 9. On the other hand, a 7-segment display is a common type of electronic display device that can show the digits 0 to 9 and some additional characters using seven individual segments.[17]

To convert a BCD digit to a 7-segment format, you map the input BCD bits to the appropriate outputs of the decoder. For example, if the BCD input is 0000, the decoder will activate the segments corresponding to the digit 0. If the BCD input is 0101, the decoder will activate the segments corresponding to the digit 5.

The specific mapping between BCD inputs and 7-segment outputs depends on the implementation of the decoder. Different decoders may have slightly different arrangements of the output signals. However, in most cases, the mapping is designed to provide a logical and intuitive representation of the decimal digits on the 7-segment display.[17]

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Hex Number	Common-Anode	CA	CB	CC	CD	CE	CF	CG	Cathode[6:0]
0	high	low	low	low	low	low	low	high	0000001
1	high	high	low	low	high	high	high	high	1001111
2	high	low	low	high	low	low	high	low	0010010
3	high	low	low	low	low	high	high	low	0000110
4	high	high	low	low	high	high	low	low	1001100
5	high	low	high	low	low	high	low	low	0100100
6	high	low	high	low	low	low	low	low	0100000
7	high	low	low	low	high	high	high	high	0001111
8	high	low	low	low	low	low	low	low	0000000
9	high	low	low	low	low	high	low	low	0000100
a	high	low	low	low	low	low	high	low	0000010
b	high	high	high	low	low	low	low	low	1100000
c	high	low	high	high	low	low	low	high	0110001
d	high	high	low	low	low	low	high	low	1000010
e	high	low	high	high	low	low	low	low	0110000
f	high	low	high	high	high	low	low	low	0111000

Fig. 5: Result of BCD to Seven segment

To convert BCD to a 7-segment display format, you need a BCD to 7-segment decoder. This decoder is a combinational logic circuit that takes a BCD input and produces the appropriate combination of signals to illuminate the corresponding segments of the 7-segment display.

A typical BCD to 7-segment decoder has four inputs, labelled A, B, C, and D, representing the four BCD bits. These inputs can have binary values from 0000 to 1001, which correspond to decimal digits 0 to 9. The decoder also has seven outputs, labelled a, b, c, d, e, f, and g, which are connected to the individual segments of the 7-segment display.

Each output of the decoder is associated with a particular segment of the display. The segments are usually labelled a through g, where a, b, c, d, e, f, and g represent the segments that form the numerical digits.

III. RESULTS AND CONCLUSION:

After compilation the VHDL code we can generate waveform from the code. From the wave we will know about our exertion is working or not. We add input output pins in the wave as shown as below.

Subsequent to doing study on computerized car parking system it is discovered that robotized car parking systems can be presented in our country and it will be recipient with regards to our country. The primary advantages are time and diminish congested driving conditions. It can likewise give supportable stopping the board in an ecoaccommodating way. As the Green House Gas outflow will be less in sum and the environment will be spotless. There is less support cost for this framework so it is helps the property designer in cost sparing. It gives security to the parking ground. Computerized car parking systems lessen the issue in parking grounds and road turned parking lot. It will profit the property designer to build their income which will add to the administration impose income. So, in a way it is

additionally helping the administration by expanding charge income. It will likewise empower Automation Engineering in our country which will make progression in expanding use of innovation. In this manner we ought to present computerized car parking systems and appreciate the advantages.

REFERENCE

[1]. Ramneet Kaur and Balwinder Singh," design and implementation of carparking system on fpga" International Journal of VLSI design & Communication Systems (VLSICS) Vol.4, No.3, June 2013.

[2]. Khor Jing Yong and Muataz H. Salih," Design and implementation of embedded auto car parking system using FPGA for emergency conditions", Indonesian Journal of Electrical Engineering and Computer Science Vol. 13, No. 3, March 2019, pp.

[3]. Bhavana Chendika, Alapati Manideepu and Fazal Noorbasha," Implementation of Secured Car Parking Management System Using Verilog HDL", Int. Journal of Engineering Research and Applications, Vol. 13, No. 3, March 2019, pp. 876~883.

[4]. S.Sharmila Devi, Blessy Angel J.J.R.,Deepa. and M., Kaaviya.A.I., "Car Parking System Using FPGA", International Research Journal on Advanced Science Hub (IRJASH),Vol.02, No.8, August 2020.

[5]. M. M. Rashid, A. Musa, M. Ataur Rahman, and N. Farahana, A. Farhana, "Automatic Parking Management System and Parking Fee Collection Based on Number Plate Recognition", International Journal of Machine Learning and Computing, Vol. 2, No. 2, April 2012

[6]. Hua-Chun Tan; Jie Zhang; Xin-Chen Ye; Hui-Ze Li; Pei Zhu; Qing-Hua Zhao;(2009) , "Intelligent carsearching system for large park," International Conference on Machine Learning and Cybernetics, 2009 , vol.6, pp.3134-3138.

[7]. Rehanullah Khana, Yasir Ali Shahb, Zeeshan Khanc, Kashif Ahmedad, Muhammad Asif Manzoorc, Amjad Alia, "Intelligent Car Parking Management System On FPGA", IJCSI International Journal of Computer Science Issues, Vol. 10, Issue 1, No 3, January 2013, ISSN (Print): 1694-0784 | ISSN (Online): 1694-0814.

[8]. Azeem Mohammad Abdul, B,Mmurali Krishna, K.S.N Murthy, Habibulla Khan, M.Yaswanth, G.Meghana and G.L. Madhumati," IOT Based Home Automation Using FPGA",Journal Of Engineering and Applied 1937,2016.

[9]. Prasanna S. Bhoite and Madan B. Mali," Wireless Signal Transmission using an Android Mobile and FPGA", International Journal of Advanced Communication Engineering Vol. 5, Issue 5, May 2016.

[10]. Devchandra Singh and Dr Manoj Kumar, "Design and development of bluetooth based home automation system using FPGA",IJAER, Vol.16,no.10,2021.

[11]. http://dspace.daffodilvarsity.edu.bd:8080/bitstream/handle/123456789/318/P12854%20%2837%25%29.pdf?sequence=1&isAllowed=y

[12]. https://www.fpga4student.com/2017/08/car-parking-system-in-vhdl-using-FSM.html

[13]. https://www.ripublication.com/ijaer22/ijaerv17n3_01.pdf

[14]. https://www.xilinx.com/products/boards-and-kits.html

[15]. https://www.xilinx.com

[16]. www.altera.com

[17]. https://www.fpga4student.com/2017/09/seven-segment-led-display-controller-basys3-fpga.html